L Number	Hits	Search Text	DB	Time stamp
1	87	(nonvolatile or non-volatile or "non volatile") and "common source line" and "source transistor" and select$3 and well and substrate	USPAT; US-PGPUB	2002/11/01 15:53
2	27	((nonvolatile or non-volatile or "non volatile") and "common source line" and "source transistor" and select$3 and well and substrate) and isolat$3	USPAT; US-PGPUB	2002/11/01 15:53

L Number	Hits	Search Text	DB	Time stamp
1	148	(nonvolatile or non-volatile or (non adj volatile)) and (common adj source) and (split adj gate)	USPAT; US-PGPUB	2002/11/01 11:39
2	101	((nonvolatile or non-volatile or (non adj volatile)) and (common adj source) and (split adj gate)) and row and column	USPAT; US-PGPUB	2002/11/01 11:40
3	82	(((nonvolatile or non-volatile or (non adj volatile)) and (common adj source) and (split adj gate)) and row and column) and (source adj line)	USPAT; US-PGPUB	2002/11/01 11:40
4	45	((((nonvolatile or non-volatile or (non adj volatile)) and (common adj source) and (split adj gate)) and row and column) and (source adj line)) and (select$3 adj transistor)	USPAT; US-PGPUB	2002/11/01 13:03
5	1	6400603.pn.	USPAT; US-PGPUB	2002/11/01 11:42
6	1	5949718.pn.	USPAT; US-PGPUB	2002/11/01 13:03
7	9	5949718.uref.	USPAT; US-PGPUB	2002/11/01 13:03

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device 10 shown in FIG. 1. FIG. 3 is a cross-sectional view of the non-volatile semiconductor memory device 10 taken along a line A--A shown in FIG. 2, and FIG. 4 is a cross-sectional view of the non-volatile semiconductor memory device 10 taken along a line B--B shown in FIG. 2.

(9) The non-volatile semiconductor memory device 10 has a NOR type memory cell array structure in which a plurality of memory cells are connected in parallel to bit lines.

(10) As shown in FIG. 2, the non-volatile semiconductor memory device 10 further includes insulation regions 5, insulation regions 5X, and bit line contacts 6a and 6b. For example, the isolation region 5X is positioned between the source lines SL2 and SL3 adjacent to each other. Therefore, the adjacent source lines are electrically independent from each other. The isolation regions 5 and the isolation regions 5X are formed by LOCOS (Local Oxidation of Silicon), STI (Shallow Trench Isolation), etc. However, other methods may be used.

(11) Hereinafter, a write method and an erase method of the non-volatile semiconductor memory device 10 will be described with reference to FIG. 5.

(12) FIG. 5 shows a threshold voltage distribution diagram of memory cells in the non-volatile semiconductor memory device 10. In FIG. 5, the abscissa represents a threshold voltage V.sub.TM of the memory cells, and the ordinate represents the number of memory cells.

(13) It is assumed herein that the non-volatile memory device 10 is a mask ROM composed of N-type MOS transistors having two difference threshold voltages.

(14) An erase state ("E" state in FIG. 5) refers to that N-type MOS transistors are set at a threshold voltage (lower threshold voltage) of about -1 volt, in which the N-type MOS transistors are in a depletion state. An erase state can be controlled by ion implantation to the channel portions of memory cells in the entire memory array.

(15) A write state ("W" state in FIG. 5) refers to that ions are additionally

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plurality of first conductivity type wells extending in the row direction, wherein one of the plurality of memory cells is a MOS transistor having a gate electrode, a gate insulating film, a drain region, and a source region on one of the plurality of first conductivity type wells, and each of the plurality of first conductivity type wells is electrically independent.

(32) The above-mentioned non-volatile semiconductor memory device includes a plurality of first conductivity type wells extending in the row direction, wherein one of the plurality of memory cells is a MOS transistor having a control gate electrode, a floating gate electrode, a gate insulating film, a drain region, and a source region on one of the plurality of first conductivity type wells, and each of the plurality of first conductivity type wells is electrically independent.

(33) A method for driving the above-mentioned non-volatile semiconductor memory device, in which information is read from a memory cell selected from the plurality of memory cells, includes the steps of: applying a first voltage having a polarity which is reverse-biased with respect to the semiconductor substrate to a bit line corresponding to the selected memory cell; applying a second voltage having the same polarity as a polarity of the first voltage to a word line corresponding to the selected memory cell; applying a third voltage having the same polarity as a polarity of the first voltage to a source line corresponding to memory cells other than the selected memory cell; and applying an electric potential of the semiconductor substrate to a source line corresponding to the selected memory cell.

(34) In one embodiment of the present invention, the first voltage and the third voltage have substantially the same.

(35) A method for driving the above-mentioned non-volatile semiconductor memory device, in which information is read from a memory cell selected from the plurality of memory cells, includes the steps of: applying a first voltage having a polarity which is reverse-biased with respect to the semiconductor substrate to a bit line corresponding to the selected memory cell; applying a second voltage having a polarity identical with a polarity of the first voltage to a word line corresponding to the selected memory cell; applying a third voltage having a polarity opposite to a polarity of the first voltage to a

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